circuit **62**. At the same time, the control circuit **63** generates certain assumed values for bits b(x) thru b(x−K+1) on the conductors **65***c* which also go to the metric circuit **62**. Then, circuit **62** evaluates the metric of FIG. **4** using the particular values for the various terms that are on the conductors **65***b*, **65***c*, and **65***f*. That result is generated on conductor **65***d* where it is received by the control circuit **63**. Circuit **63** utilizes the metric on conductor **65***d* to update a stack in memory **64** in accordance with the sequence shown and described in FIGS. **5** and **8**. Circuit **63** then compares the stack entries to determine which has the largest metric and its corresponding bit sequence. Based on that determination, circuit **63** then generates a new index of "x" and new bits b(x) thru b(x-K+1) on conductors **65***f* and **65***c* respectively.

Considering now FIG. **10**, it shows the details of the metric circuit **62**. One section of this circuit is comprised of a register **71** which has K−1 stages, a memory **72** which stores the autocorrelation functions H(x,x+1) thru H(x,x+K−1), a set of K−1 multipliers **73**, an adder **74**, and another multiplier **75**. All of these components are interconnected as illustrated, and they operate to generate the term $I_f(x)$ in the FIG. **4** metric.

Another section of the FIG. **10** circuit includes a one-stage register **81**, and a multiplier **82**. Those components are interconnected as illustrated, and they generate the term $2b(x)y(x)$ of the FIG. **4** metric.

Another section of the FIG. **10** circuit includes a memory **91** which stores the power level of the individual bit sequences in the composite signal, and a pair of multipliers **92** and **93**. Components **91–93** are interconnected as illustrated, and they form the term $b^2(x)w(x)$ of the FIG. **4** metric.

Further included in the FIG. **10** circuit is a register **101** which has K−1 stages, a memory **102** which stores the autocorrelation functions H(x,x−K+1) thru H(x,x−1), a set of K−1 multipliers **103**, an adder **104**, and another multiplier **105**. All of these components **101–105** are interconnected as illustrated, and they form the term $I_p(x)$ in the FIG. **4** metric.

In operation, the controller **63** generates assumed values for bits b(x) thru b(x−K+1) on the leads **65***c*, and the matched filters **61** generate actual filter outputs for bits b(x) thru b(x+K-**31** 1) on the leads **65***b*. Those values are then operated on by components **71** thru **75**, **81** thru **82**, **91** thru **93**, and **101** thru **105** to form the above described metric terms. Circuit **110** combines those terms, as well as the noise term N_o1n2, in accordance with FIG. **4**; and it sends the resulting metric M_x to the control circuit **63** on the leads **65***d*.

A preferred process of decoding bits in a composite signal in accordance with the invention, as well as circuitry for carrying out that process, have now been described in detail. In addition, however, many changes and modifications can be made to those details without departing from the nature and spirit of the invention.

For example, many suitable implementations of the matched filters exist. One such implementation consists of a two input multiplier and a one input integrator for each filter. Signal c(t) goes into one of the multiplier inputs; the spreading code of a particular transmitting station goes into the other multiplier input; the multiplier output goes to the integrator input; and the output of the integrator is the matched filter output.

Also in the disclosed process, several modifications can be made to the FIG. **4** metric. For example, in the FIG. **4** metric the term $I_f(x)$ compensates for the interference to bit b(x) which is caused by the next successive K−1 bits in the composite signal. But, as the amount of correlation between the spreading codes for bit b(x) and a successive bit decreases, the amount of interference also decreases. Consequently, one or more of the terms [sign y(x+i)H(x,x+i)] which have the smallest correlations H(x,x+i) can be dropped from the interference term $I_f(x)$ in order to simplify the metric, at the risk of increasing the errors that occur in the decoding procedure.

For example, consider the leftmost column in FIG. **7** which shows the correlations H(x,x+i) where bit b(x) comes from station T_1. There, H(x,x+2) is $1.94x10^{-2}$, whereas H(x,x+3) is almost ten times larger. Consequently, the term [sign y(x+2)H(x,x+2)] in the FIG. **4** metric can be dropped whenever bit b(x) is from station T_4.

Similarly, one or more of the terms b(x−i)H(x,x−i) can be dropped from the interference term $I_p(x)$. For example, the rightmost column of FIG. **7** shows that a relatively small correlation exists between the spreading codes of bits b(x) and b(x−2); and thus the term b(x−2)H(x,x−2) can be dropped from the FIG. **4** metric whenever b(x) is from station T_4.

Further, the constants by which the interference terms $I_p(x)$ and $I_f(x)$ are multiplied in the FIG. **4** metric can be increased or decreased to modify the relative weight or importance of the terms in the decoding process. In addition, the noise term $-N_o1n2$ in the FIG. **4** metric can be modified. For example, by changing it to $d_{min}-W(x)\ -N_o1n2$ where d_{min} is the minimum distance between the various spreading codes of the transmitting stations, fewer decoding errors will occur in the case in which multi-user interference is strong (i.e., where $d_{min} <$MIN W (x)).

Accordingly, it is to be understood that the invention is not limited to the above details, but is defined by the appended claims.

What is claimed is:

1. A method of decoding superimposed data bits including the steps of:

receiving a composite signal that is formed by coding multiple bit sequences with respective spreading codes and transmitting the coded bit sequences simultaneously and asynchronously over a single channel;

comparing the content of several registers, each of which contains an estimate of a particular bit sequence in said composite signal and a metric for that sequence, to determine the largest metric M_{max} and the corresponding bit sequence b_s;

evaluating a new pair of metrics for the very next bit b(x) in said composite signal which follows said bit sequence b_s by using estimated "0" and "1" values for bit b(x), bits from said sequence b_s which immediately precede bit b(x), and matched filter outputs for bits in said composite signal which immediately follow bit b(x);

replacing the register which contains said bit sequence b_s with two registers, one of which contains the bit sequence b_s b(x)=0 and the metric M_{max} plus the above evaluated metric for b(x)=0, and the other of which contains the bit sequence b_s b(x)=1 and the metric M_{max} plus the above evaluated metric for b(x)=1;

repeating said comparing, evaluating, and replacing steps multiple times; and thereafter,